# LP3991TL micro SMD Evaluation Board Information

National Semiconductor
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## Introduction

This board is designed to allow the evaluation of the LP3991 Low Voltage CMOS Regulator. Each board is pre-assembled and tested in the factory. The board contains the LP3991 in a 4 bump micro SMD package and input and output capacitors connected to GND . The LP3991 is capable of operating with an input voltage as low as 1.65V for output voltage options of 1.5V or less. The LP3991 can supply a maximum output current of 300mA and is particularly suitable for powering digital circuits, where good transient behavior is required. It can be employed in applications requiring post regulation of switching regulators to provide maximum efficiency in battery powered products.

## Operation

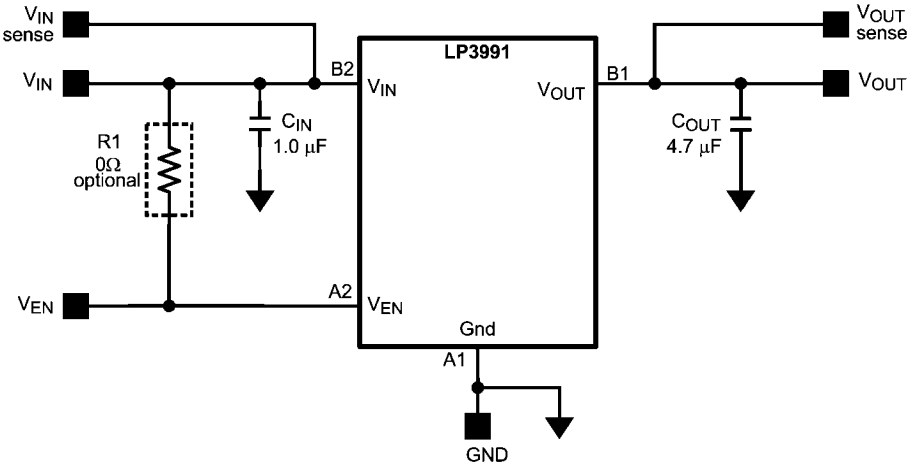
The input voltage, applied between $V_{IN}$ and GND should be at least 0.5V above the output voltage with a minimum of 1.65V and a maximum of 3.3V. For output voltages of 1.5V or higher, the LP3991 will operate with an input voltage of only 0.2V above $V_{OUT}$. However, some loss in performance of PSSR and transient behavior can be expected when operating the device with such a low $V_{IN}$ to $V_{OUT}$ difference. Input connections should be kept reasonably short (<300mm) to minimize input inductance and ensure optimum transient performance. If longer leads are used, then it may be required to increase the input capacitor value to 2.2µF or 4.7µF.

ON/OFF control of the LP3991 is provided on the evaluation board by a logic signal applied to the $V_{EN}$ pin. A minimum of 0.95V is required to guarantee the device to be on and the device will be shutdown with $V_{EN}$ set to 0.4V or less. If ON/OFF control is not required, the $V_{EN}$ pin can be connected to $V_{IN}$. The evaluation board has provision for an optional link (R1) for this purpose.

A load may be connected from the $V_{OUT}$ pin to GND.

The schematic and board layout are shown below:

## Schematic Diagram

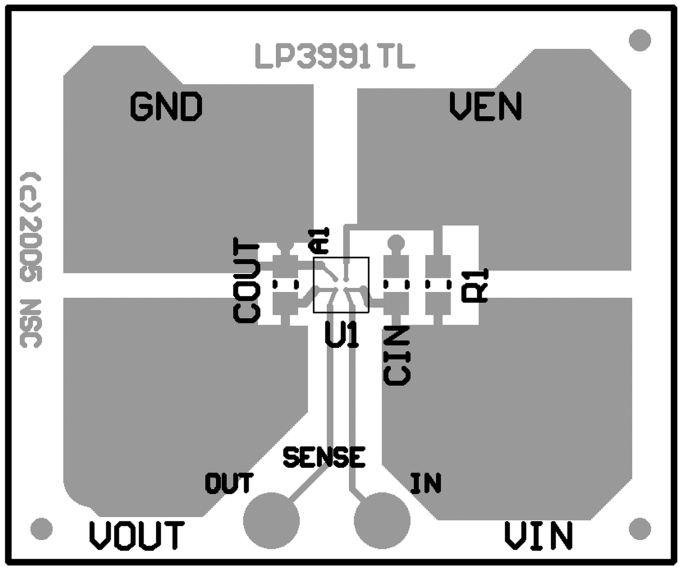



**Evaluation Board Schematic**



## PCB Layout

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**Evaluation Board Component and Pin Layout**
**Board Size:- 1.200" X 1.000"**

## Bill of Materials for LP3991 Micro SMD Evaluation Board

| Item | Value | Qty | Footprint | Notes |
|---|---|---|---|---|
| U1 | LP3991SD-X.X | 1 | TLA-04 | "X.X" corresponds to the output voltage option. |
| $C_{IN}$ | 1.0µF | 1 | 0603 | X5R, Input Capacitor |
| $C_{OUT}$ | 4.7µF | 1 | 0603 | X5R, Output Capacitor |
| R1 | 0Ω | Not Fitted | 0805 | Connects $V_{IN}$ to $V_{EN}$ |
| Test Pins | | 4 | | |

# Notes

# Notes



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